Reliability simulation in CMOS 90nm design using Eldo

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Introduction

- Aggressive device performances are required in modern CMOS technologies
  - SoC, multiple devices → less degrees of freedom
  - Overdrive / unscaled Vdd : more performances expected
- Reliability margins better quantified, but are narrower than before
- Exhaustive OLT (Operational Life Test) of final product is quite difficult
  - Products are convergence driven
    - difficult to optimize OLT with respect to planning, execution and costs
    - expensive to correct any reliability problems occurring at this level.
- Intrinsic reliability : move from management at process level towards a « process/design » co-management
- NBTI is a new limiting failure mode for modern technologies which requires this co-management intrinsic reliability
Goal of this presentation

- To present an open solution for reliability assessment developed within a circuit simulator (Eldo from Mentor Graphics)
  - To discuss some of the features that are useful in translating different issues of device reliability for the actual circuit operating conditions.
- To present its application to NBTI degradation in 90nm technology
Reliability simulation

- Spurt of DiR (Design in Reliability) tool development during early 1990’s, in universities (UC,Berkeley[1], UI,Urbana-Champaign[2], University of Southern California[3], as well as a few companies (TI[4], Philips[5]) lead to automated tools to check intrinsic reliability.
  - Hot-carrier, gate oxide, electro migration issues
    - Targeted at small circuits.
  - Activity on further development decreased during the late 90’s
    - In part due to perception of effective reliability control at technology level.
  - Usage of these tools typically confined to specific groups
  - Detailed analysis of tools can be found for example in [6].
Reliability simulation

- Advanced technologies and newer aging issues (such as NBTI [7]) have recently renewed interest amongst both technology and design communities to have a DiR solutions.

- **Increasingly, there is a push to have reliability analysis methodology integrated into the design flow.**
  - Designers increasingly aware and uncomfortable with reducing reliability margins
    - Seek more quantitative and relevant reliability guidelines.
    - Tools preferred where available.
Reliability simulation integration into design methodology

- Robustness and integration into SPICE models.
  - SPICE is the sole representative of the actual device that a designer has.
    - Many physical effects have begun to be packed within SPICE definition (Process corners, mismatch, mechanical stress, ...)
  - The device model parameter definition is quite complex
    - Uses subcircuits
    - Actual parameters are derived from several interlinked coefficients
  - The coefficients associated to reliability are an additional but independent part of SPICE model
    - Enable simulation with or without reliability
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Reliability simulation – Flow

Extended model card

Standard BSIM model

Reliability model (Eldo UDRM)

Reliability parameters

Description of Transistor Stress as function of Activity

Description of BSIM parameters evolution as function of Stress

Extra object Library

Netlist

Model Parameters (Fresh)

Aging related commands

Eldo

Stress analysis

Simulate Fresh

Simulate Aged

Updated BSIM3/4 parameters

Stress File

Optional

Nominal Results

Aged Results

Comparison

.Netlist

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Sample commands:

.AGE [TAGE=value]
+ [TSTART=value] [TSTOP=value]
+ [MODE=AGEsim | AGEload | AGESave] [AGBLIB=file_name]
+ [AGEALL=[YES|ON|1]|{NO|OFF|O}]
+ [ASCIIT=[YES|ON|1]|{NO|OFF|O}]
+ [COMPUTE_LAST=[YES|ON|1]|{NO|OFF|O}]

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Stress assessment – 1/3

☐ Minimal overhead for the designer
  - Ease of use: just add the .AGE command
  - Minimum CPU time impact using on-the-fly processing
    • No need to store large amounts of data
    • No separate time required for reliability analysis.

☐ Eldo UDRM (User Defined Reliability Model)
  - Flexible modeling: model implemented via an API and compiled into an Eldo dynamic library
  - models can be updated with the latest developments on the physics/experimental front
    • Important, since the physical understanding of the phenomenon such as NBTI is continuously evolving
      ▪ Saturation after long durations of stress
      ▪ AC effects
      ▪ Spice Degradation components, etc
Eldo UDRM API - access functions

- The API provides read access functions to:
  - instance parameters (W, L…)
  - usual quantities (Vdsat, Vth, Isub…)
  - parameters of the stress model (user defined, unlimited)
  - parameters of the “parameter update model” (user defined, unlimited)
  - global variables (simulation time, temperature…)

- and read/write access functions to:
  - model parameters (VTH0, U0…)

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Eldo UDRM API - required functions

- User-defined functions required to fully define an aging mechanism:
  - register parameter names and default values for the stress model
  - register parameter names and default values for the “parameter update model”
  - define the equations of the stress model (Eldo handles the integration automatically)
  - define the equations of the “parameter update model”
Stress assessment – 2/3

- During reliability simulation, the device parameter evolutions are computed according to the operating condition, and the transistor is simulated with the modified SPICE parameter set to represent degradation.

**Working Principles**

LINEARIZATION

INTEGRATION

The “Stress” is modeled linearly with respect to “t” - ease of integration

Degradation(t) = (Stress)^n

Stress = \frac{\text{Age}}{T} \int_{0}^{T} f(\text{operating conditions}) \, dt

where T is the time of the unit simulation, and Age is the desired time for the reliability simulation.
Stress assessment – 3/3

- Limitless number of stress vectors
  - Can be used to store additional data during the stress analysis

  • Stress analysis can be made more complete and closer to the physical reality by storing some important information during the stress assessment for later sets of simulation runs
    ▪ The second set of simulations (performance impact assessment) are entirely independent from the first simulation, except for the stress file.
    ▪ By storing the conditions of stress, certain decisions can be made during the second simulation run
      e.g., saturation of degradation
During the subsequent simulation run(s), the BSIM3 or BSIM4 model parameters specified through the UDRM are updated to reflect the characteristic of the aged device.

- Flexibility in analysis: the subsequent simulation can be in a different operating mode than the first simulation via the stress file loading.
  - The calculated stress is stored in a simple file and can be used for multiple “aged” simulations.
  - For designers, it is helpful to assess performances in different modes of the circuit.
  - For reliability model developer, it helps to verify impact of model parameter update.
Negative Bias Temperature Instability

- NBTI – is a DC stress
  - Without any requirement of mobile carriers
  - Proportional to applied Vgs and Temperature
  - Causes uniform degradation across the oxide interface
  - Causes change mainly in the linear parameters (Vth and mobility related parameters)
  - No geometry dependence
  - Phenomenon complicated with evolving findings with respect to mechanism, behavior and model [8,9]
  - The details of the simpler version of the NBTI model spelt out here.

\[
\Delta D = \beta \cdot e^{\gamma Vgs} \cdot e^{-\frac{Ea}{kT}} \cdot L^m \cdot t^n
\]

**Integral form**

\[
\text{Stress} = N \int_0^T (\beta \cdot e^{\gamma Vgs} \cdot e^{-\frac{Ea}{kT}} \cdot L^m)^{1/n} dt
\]

**Spice Parameter update**

\[
\Delta P = C \cdot (\text{Stress})^n
\]
NBTI degradation simulation

- Vth is used to monitor the degradation
- Parameters seen to change (depending on device family)
  - Vth, u0, ua, nfactor
  - Saturation regime changes as well as length dependence seen to arise directly from the changes in the above parameters
Example of simulation results

Buffer - Delay Increase

IO Input - Threshold change
Conclusion

- Eldo UDRM – an open model for reliability simulation
  - Scope to include effects arising due to specificity of degradation
    - Relaxation
    - AC effects
    - Long term saturation

- Implementation for different device families from the 90nm node onwards at ST
  - Designers can now quantify the reliability assessment of circuit blocks.

- NBTI model evolving. Interface open to consider the new effects.
Bibliography