MOSFET breakdown and snapback modelling for ESD protection design in the state of the art CMOS

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ESD is a serious reliability problem for the IC’s

CMOS input gates:
- oxide breakdown

output buffers:
- drain-substrate junction breakdown
- power dissipation

internal chip issues
- as \( V_{dd} \) to \( V_{ss} \) current path
- and more ...

ESD acts as a current source!

\[ I_{ESD} \sim [A], \quad t_{ESD} \sim [ns] \]
OBJECTIVES

Development of a simulation based ESD protection design methodology:

- ESD valid models for the state-of-the-art MOSFETs
- Parameter extraction procedures
- Integration in a common design environment
- Circuit level ESD protection optimization
The purpose is to limit the voltages that appear at the various circuit nodes and to route the ESD current through a “known path”.
NMOS - the core clamp in CMOS

INTRODUCTION

- easy to integrate (also for self-protection !)
- different configurations to improve the ESD properties - gate grounded; gate or substrate coupled
- CMOS technology ESD benchmark device

lateral NPN bulk transistor active in ESD

Important for the ESD regime

100ns TLP I/V snapback characteristics

OUTLINE

INTRODUCTION

IMPACT OF THE TECHNOLOGY SCALING ON THE MOSFET BREAKDOWN AND SNAPBACK

THE ADVANCED MOSFET SNAPBACK MODEL

PARAMETER EXTRACTION

APPLICATION TO ESD CIRCUIT OPTIMIZATION

CONCLUSIONS
Major ESD model requirements

Description of the MOSFET snapback operation – I(t), V(t)
(accuracy ΔV/V ~ 10-30%, ΔI/I<10%, determined by the ESD design space)
Scalability with the major ESD design parameters - W,L,SWS,SB
Applicability for I/O pad cell level simulations (efficiency, convergence)

Physical effects to be considered:
• MOSFET breakdown
• Bipolar triggering
• Bipolar operation
• High-current conduction

Not significant from ESD circuit operation design view
• self-heating and elevated T₀ operation
• failure level modelling

Impact of the CMOS technology on the junction breakdown

The CMOS downscaling leads to:
Reduced avalanche breakdown voltage
Increased tunneling leakage currents
Less importance of the high-injection effects

Additional models beside avalanche need to be considered to describe the junction reverse bias conduction!
Impact of the CMOS technology on the junction breakdown behaviour: effects of the drain-gate field

The breakdown of the NMOS (i.e. gated N+/P\text{well} junction) is becoming increasingly dependant on the gate field!

Impact of the CMOS technology on the junction breakdown behaviour: effects of the drain-gate field

- at low $V_{\text{GD}}$ (i.e. high drain-gate vertical field)
  \[ 2V_{\text{BR, MOS}} - V_{\text{BR, diode}} \sim V_G \]

- at high $|V_{\text{GD}}|$ (i.e. low drain-gate vertical field)
  \[ 2V_{\text{BR, MOS}} - V_{\text{BR, diode}} \sim V_{\text{BR, diode}} \]

using the empirical model

\[ 2V_{\text{BR, MOS}} - V_{\text{BR, diode}} \sim V_{\text{BR, diode}} \]

\[ = V_{\text{BR, diode}} - V_{\text{BR, diode}} \]

\[ - q_0 L_B \left[ 1 + e^{-\frac{V_G - (V_{\text{BR, diode}} - V_{\text{BR, diode}})}{\epsilon}} \right] \]

Modeling the breakdown voltage dependence on the gate bias is needed to describe the observed ESD behaviour of the MOSFET
ESD model topology and basic equations

Equivalent circuit model (to ease the practical implementation)
- Analog HDL implementation of the equation defined current/potential generation sources
- Symmetrical topology for D/S (Important for variable polarity ESD stress e.g. CDM)
- Capacitance model—the same as for the intrinsic MOSFET

Accurate description of the actual physics and the observed ESD behaviour can be achieved
ESD model topology and basic equations

Current generation sources

\[ I_{arc} = (M_b - 1) I_c + M_b I_{gen} \]

\[ I_{arch} = (M_{ch} - 1) I_{ch} \]

- \( I_{c}, I_{ch} \): self-consistently calculated
- \( I_{gen} = I_{BTBT} + I_{TAT} \): generated by the high field tunneling currents

\[ I_{TAT} = A_t \left| E_m \right|^n e^{\frac{E_m}{B_{ref}}} \]

\[ I_{BTBT}(E_m^{vert}) = A_{bt} \left| E_m \right|^n e^{\frac{E_m^{vert}}{B_{ref}}} \]

Avalanche multiplication factors

(modified Miller expressions)

\[ M_b = \frac{V_{BB} - c_{diff} V_{BD}}{V_{BB} - c_{diff} V_{BD}^M} + 1, \]

\[ M_{ch} = \frac{V_{BB} - c_{diff} V_{BD}^M}{V_{BB} - c_{diff} V_{BD}} + 1, \]

- \( V_{BB}, V_{DB} \): calculated by the model
- \( V_{DD} \): from the channel current model
- \( V_{BR}^{MOS} = V_D \cdot E_m \cdot E_{crit} \): a semi-empirical model that is function of \( V_G \), extracted from the measurements
- \( k_m, n \): extracted, \( c_{diff}, c_{vsat} \): fitted

Typical comparison with experiments

Quasistatic snapback I/V

ESD time domain operation

Human Body Model ESD stress
Analog Artist/CADENCE INTEGRATION

• implementation in the standard CADENCE PDK environment
• SPECTRE&HSPICE simulation
Parameter Extraction

The intrinsic MOSFET – a library model
Extraction of the bipolar parameters as function of the ESD layout variables
- multiplication factors $M_b, M_{ch}$
- substrate potential and tunneling sources
- current gain $\beta$
- high current ‘on’ resistance
- base transit time

Scaling of the parameters - based on physically based semi-empirical expressions

The ESD model parameters are extracted from an array of structures using reverse solutions of the model equations (whenever possible) and applied to representative parts of the experimental characteristics.

Illustration of the 2-step self-consistent extraction of the breakdown and substrate tunneling currents models (the resistive behaviour model after breakdown and the high-current conduction are extracted separately)
Parameter Extraction

\[ R_{\text{ON}} = c_0 + c_1 \frac{(SB + CI)}{W} \]

Extraction of the scaling behaviour of the ESD high current resistance \( R_{\text{ON}} \)

IC-CAP implementation of the extraction methodology

- Direct extraction (using custom macros) & fine tuning of the parameters (using the IC-CAP tuner and optimizer)
- Both the static and transient ESD behaviour of the device can be represented in IC-CAP

IC-CAP is a standard tool for the industry
- Fully compatible with the standard MOSFET extraction implementation
- Issues to be resolved with the LOG current sweep required for the snapback simulations
Application Examples: Multifinger device triggering

Due to the different substrate resistance of the multifinger NMOS, finger non-uniform ESD conductance can be established, which has to be avoided in the protection design.
Application Examples: Output Pad Cell protection optimisation

The triggering of the devices in ESD conditions can be optimised by simulations. Here, a gate coupled (gc) protection NMOS (not shown) was used to deviate the stress current from the driver NMOS.

Application Examples: Power Pad Cell behaviour optimisation

Good correlation between the measured and simulated circuit behaviour under ESD conditions is typically observed at I/O pad cell level.
CONCLUSIONS

The MOSFET operation under ESD stress requires to consider some specific physical effects. The extension of the standard library MOSFET models to models valid under ESD stress was shown to be possible and was verified for CMOS technology devices ranging from 0.5μm down to 90nm.

Employing a good CAD based ESD design methodology allows to understand and optimise the device and circuit behaviour in a faster and much more reliable approach, not using any black magic.
In a company close to you…

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