A Scalable Advanced RF IC Design-Oriented MOSFET Model

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ABSTRACT: This article presents a validation of the EKV3 MOSFET compact model dedicated to the design of analogue/RF ICs using advanced CMOS technology. The EKV3 model is compared with DC, CV and RF measurements up to 20 GHz of a 110 nm CMOS technology. The scaling behaviour over a large range of channel lengths and bias conditions is presented. Long-channel devices show significant non-quasi static effects while in short-channel devices the parasitics modelling is critical. This is illustrated with Y-parameters and $f_t$ vs. $I_D$ in NMOS and PMOS devices, showing good overall RF modelling abilities of the EKV3 MOSFET model.

Keywords: MOSFET; compact model; analogue/RF IC design; RF modelling; NQS effect; scaling

I. INTRODUCTION

The key to designing analogue/RF integrated circuits in advanced CMOS technology [1] lies in successfully trading-off design constraints, such as power consumption, supply voltage, noise, linearity, gain, etc [2]. The circuit simulation model of the MOS transistor should predict electrical behaviour including noise over a very wide range of geometry, bias, temperature and frequency [3, 4]. Non-quasi static (NQS) effects [5] occurring in the intrinsic channel may affect particularly long-channel devices and even more importantly in weak inversion, while extrinsic parasitic elements are particularly important for short-channel devices [6]. Although significant effort has been deployed over the last years to develop scalable RF MOSFET compact models for circuit simulation, it is very rare that their validity is shown simultaneously over a wide range of the above aspects. In the present work, a consistent and extended validation of the recently available charge-based EKV3 [7] MOSFET model will be presented.

The present study is based on a 110 nm CMOS technology featuring a triple well with shallow-trench isolation (STI), with multi-$V_{TH}$ MOSFETs at 1.5 V/2.5 V. The gate and source-drain use Co-silicidation while the oxide uses oxynitride as an insulator. The channels are halo-implanted as shown in Figure 1. Further detail of device fabrication may be found in [8–10].

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Available devices for RF characterization are NMOS and PMOS type transistors within a classic multi-finger layout as shown in Figure 2. Gate lengths considered in the present work range from $L_f = 110 \, \text{nm}$ to $2 \, \text{μm}$, with a fixed finger width $W_f = 5 \, \text{μm}$ and a number of fingers $N_f = 10$. The sources of the transistors are grounded.

The study is organized as follows. The static EKV3 charge-based model structure is first presented. High-frequency equivalent circuit and corresponding equations are introduced and the RF parasitics network is discussed. DC, CV and RF operation of the devices is then presented with emphasis on scaling over bias conditions and channel length. All aspects are illustrated equally for both NMOS and PMOS transistors.

II. STATIC MODEL: THE CHARGE-BASED EKV MOSFET MODEL

In the EKV model, the pinch-off voltage $V_P$ serves as a reference for the channel voltage. $V_P$ is conveniently expressed as [11],

$$V_P = \frac{V_G - V_{TO}}{n} = n + \frac{\gamma}{2\sqrt{V_P + \Phi}}$$

(1)

where $V_{TO}$ is the threshold voltage and $n$ the slope factor. The latter depends in turn on the body effect factor $\gamma$ and (twice) the Fermi potential $\Phi$. Inversion charge at source and drain $q_s$ and $q_d$ are related to the quantities $V_P - V_S$ and $V_P - V_D$, respectively, as [12, 13]

$$\frac{V_P - V_S}{U_T} = 2q_s + \ln q_s$$

$$\frac{V_P - V_D}{U_T} = 2q_d + \ln q_d$$

(2)

where $U_T$ is the thermodynamic potential. On the other hand, the drain current $I_D$ is expressed as,

$$I_D = I_{SPEC} \cdot (i_t - i_r)$$

(3)

where $I_{SPEC}$ is the so-called specific current of the device, and the forward and reverse currents $i_t$ and $i_r$ are related to the inversion charge $q_s$ and $q_d$ as,

$$i_t = q_s^2 + q_s$$

$$i_r = q_d^2 + q_d$$

(4)

In turn, the transconductances are related to inversion charges,

$$g_{ms} = q_s \frac{I_{SPEC}}{U_T}$$

$$g_{md} = q_d \frac{I_{SPEC}}{U_T}$$

$$g_m = \frac{g_{ms} - g_{md}}{n}$$

$$g_{mh} = \frac{n - 1}{n} \cdot (g_{ms} - g_{md})$$

(5)

The ratio of transconductance to current, an important design quantity in analogue circuits, is again directly related to inversion charge or forward current [12–14],

$$\frac{g_{ms} U_T}{I_D} = \frac{1}{1 + q_s} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_t}}$$

$$\frac{g_{md} U_T}{I_D} = \frac{1}{n} \cdot \frac{1}{1 + q_d} = \frac{1}{n} \cdot \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_t}}$$

(6)
a relationship which holds in saturation from weak inversion ($i_t < 0.1$) to moderate ($0.1 < i_t < 10$) and strong inversion ($i_t > 10$).

The model presented so far is ideal and does not yet include higher-order effects such as short-channel effects, nor parasitics. Of course these need to be included in the full computer simulation model. Polydepletion and quantum effects are among the fundamental effects affecting device performance [15]. Important mobility and velocity saturation effects are the cause of reduced device mobility and therefore are a significant limit for short-channel performance [7, 11]. Furthermore, other important short-channel effects affecting notably threshold voltage—namely reverse short-channel effect and drain induced barrier lowering (DIBL)—and substrate effect due to charge-sharing, as well as channel length modulation need to be considered. The halo-doping implants are indispensable to control DIBL in short-channel devices, however, they are the cause of degradation in terms of analogue performance at long channel [7]. Layout-dependent stress is finally an important source of deviation of device behaviour in advanced CMOS technology [10]. Another important parasitic effect in advanced CMOS is also gate tunnelling leakage. The EKV3 model has a comparatively low number of parameters to efficiently cope with all these effects [7].

### III. MODEL AT HIGH FREQUENCIES

High-frequency operation of MOSFETs requires above all accounting for the frequency response of the intrinsic channel—basically, a transmission line effect leading to the NQS phenomena. Figure 3 presents a general equivalent small-signal circuit of the MOSFET in NQS operation [3, 5].

The three voltage controlled current sources are characterized by three respective transadmittances $Y_m$, $Y_{ms}$ and $Y_{md}$:

$$Y_m \approx \frac{1}{1 + j \cdot \omega t_{qs}}$$

$$Y_{ms} \approx \frac{1}{1 + j \cdot \omega t_{qs}}$$

$$Y_{md} \approx \frac{1}{1 + j \cdot \omega t_{qs}}$$

$$Y_m = \frac{Y_{ms} - Y_{md}}{n}$$

The five admittances $Y_{gsi}$, $Y_{gdi}$, $Y_{gbi}$, $Y_{bsi}$ and $Y_{bdi}$ are related to each other as:

### TABLE I. Scaling Rules for Resistors in the Extrinsic Gate- and Substrate-Parasitics Network for Multi-Finger Devices

<table>
<thead>
<tr>
<th>Scaling Rule</th>
<th>$R_G$</th>
<th>$R_{SB}$, $R_{DB}$</th>
<th>$R_B$</th>
<th>$R_{DSB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\propto W_d(L_i \times N_i)$</td>
<td>$\propto 1/W_d$</td>
<td>$\propto 1/W_d$</td>
<td>$\propto L_d(W_d \times N_i)$</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3. Small-signal equivalent circuit of the NQS intrinsic MOSFET.

Figure 4. RF model of the MOS transistor with extrinsic elements for gate- and substrate-parasitics network.
\[ Y_{g_{si}} \approx j \omega C_{gsi} \cdot \frac{1}{1 + j \cdot \omega \tau_{qs}/2} \]
\[ Y_{g_{di}} \approx j \omega C_{g_{di}} \cdot \frac{1}{1 + j \cdot \omega \tau_{qs}/2} \]
\[ Y_{g_{bi}} = \frac{n - 1}{n} \cdot (j \omega C_{ox} - Y_{g_{si}} - Y_{g_{di}}) \]
where \( C_{gsi} \) and \( C_{g_{di}} \) are defined as,

\[ \frac{C_{gsi}}{C_{ox}} = \frac{q_s}{3} \left( q_s + q_d + 1 \right)^{-1} \]

\[ \frac{C_{g_{di}}}{C_{ox}} = \frac{q_d}{3} \left( q_s + q_d + 1 \right)^{-1} \]

In the above \( Y \)-parameters, a characteristic intrinsic time constant \( \tau_{qs} \) for the NQS effects is defined as [3].
which scales essentially with the square of the channel length, and inversely proportional to mobility \( \mu \) and \( U_T \). In saturation, the intrinsic time constant is,

\[
\tau_0 = \frac{L^2}{\mu U_T}
\]

\[
\frac{\tau_{qs}}{\tau_0} = \frac{1}{30} \frac{4q_s^2 + 10q_s + 12q_q + 10q_d + 4q_d^2 + 5}{(q_s + q_d + 1)^3}
\]

\[
\frac{\tau_{qs|\text{saturation}}}{\tau_0} = \frac{1}{30} \frac{4q_s^2 + 10q_s + 5}{(q_s + 1)^3}
\]
We then define a transcapacitance as,

\[ C_m = g_m \cdot \tau_{qs} \]  (12)

Short-channel devices are significantly affected by the extrinsic parasitics, mostly gate and substrate resistances and overlap and fringing capacitances. A subcircuit as shown in Figure 4 is used to represent these effects. The scaling of the parameters follows the rules shown in Table I.

Y-parameters are a convenient means to interpret a number of MOS transistor parameters [3] in terms of transconductances, transcapacitances and access resistances. Combining the preceding small-signal analysis of the intrinsic MOSFET with the effect of \( R_G \) and \( R_B \), assuming however \( R_{SB} = R_{DB} = \infty \) and \( R_{DSB} = 0 \), the Y-parameters may be expressed in the case of the 2-port configuration in saturation, as [16].

\[ \text{Figure 9.} \quad \text{Threshold voltage } V_{TH} \text{ versus channel length } L \text{ for the NMOS and PMOS transistors in saturation.} \ | V_D | = 1.5 \text{ V. Extraction of } V_{TH} \text{ is based on a current criterion } I_D = I_{TH} = W/L. \text{ NMOS: } I_{TH} = 1.6 \mu A; \text{ PMOS: } I_{TH} = 0.8 \mu A. \text{ Markers: measured data, Lines: EKV3 model.} \]

\[ \text{Figure 10.} \quad \text{CV characteristics of long} \ (L = 200 \mu m, W = 250 \mu m, M = 1) \text{ and short} \ (L = 0.11 \mu m, W = 101 \mu m, M = 4500) \text{ NMOS and PMOS transistors. Markers: measured data, Lines: EKV3 model.} \]
where the overlap and junction capacitance components are added to the intrinsic capacitances,

$$
Y_{11} \simeq \omega^2 R_g C_{gg}^2 + j\omega C_{eg} \\
Y_{12} \simeq -\omega^2 R_g C_{gg} C_{gd} - j\omega C_{gd} \\
Y_{21} \simeq g_m - \omega^2 R_g C_{gg}(C_m + C_{gd}) - j\omega(C_m + C_{gd} + g_m R_g C_{gg}) \\
Y_{22} \simeq g_{ds} + \omega^2 \left[ R_g C_{gd}(C_{gd} + g_m R_g C_{gg}) + R_b C_{bd}(C_{bd} + g_{mb} R_b(C_{bd} + C_{bs} + C_{gb})) \right] \\
+ j\omega(C_{gd}(1 + g_m R_g) + C_{bd}(1 + g_{mb} R_b))
$$

Figure 11. Y-parameters for a multi-finger NMOS transistor with $L_f = 2\ \mu m$, $W_f = 5\ \mu m$, $N_f = 10$. $(V_{G}, V_{D}) = (0.4\ \text{V}, 0.3\ \text{V})$, $(0.6\ \text{V}, 0.5\ \text{V})$, $(0.9\ \text{V}, 0.8\ \text{V})$. Markers: measured data, Lines: EKV3 model.

Figure 12. Y-parameters for a multi-finger NMOS transistor with $L_f = 0.11\ \mu m$, $W_f = 5\ \mu m$, $N_f = 10$. $(V_{G}, V_{D}) = (0.4\ \text{V}, 0.3\ \text{V})$, $(0.6\ \text{V}, 0.5\ \text{V})$, $(0.9\ \text{V}, 0.8\ \text{V})$. Markers: measured data, Lines: EKV3 model.
IV. VALIDATION FROM DC TO RF

In this Section, DC, CV and RF characteristics will be presented. Static and RF characteristics are obtained from the structures presented in Figure 2, while CV characteristics are obtained from separate standard CV characterization structures. We note that one single, scalable model is used coherently for all device characteristics, for either NMOS or PMOS devices.

\[ R_G = \frac{k}{3N_lL_g} \text{RGSH} \quad (15) \]

Static characteristics, including transfer characteristics, gate transconductance, transconductance to current ratio, output characteristics and output conductances are presented in Figures 5–8 for long and short NMOS and PMOS devices, respectively. The threshold voltage evaluated over the range of channel lengths is presented in Figure 9. Good overall fits are obtained with EKV3.

Capacitance-voltage characteristics from accumulation to inversion are presented for long and short NMOS and PMOS devices in Figure 10. Note the bias-dependent overlap capacitances appearing in the short-channel devices, as well as the correct modeling of fringing capacitances at the onset of strong inversion.
The four $Y$-parameters are evaluated versus frequency up to 20 GHz. Long ($L_f = 2 \, \mu m$) and short ($L_f = 0.11 \, \mu m$) multi-finger NMOS and PMOS devices are represented in Figures 11–14. Note that the three different bias conditions in saturation represent realistic operating conditions—covering moderate to strong inversion—for RF circuits such as a low-noise amplifier (LNA). The bias- and frequency-dependence of real and imaginary parts of $Y$ parameters are qualitatively well represented by the EKV3 model. Only the $Y_{12}$ parameter—and particularly the real part—is not ideally matched by the model. Note the small amplitude of both real and imaginary parts of $Y_{12}$ with respect to other $Y$ parameters particularly at low frequency; this should be of limited consequence to design. Experimental difficulties may in part also be responsible for this fact.

Long-channel devices are clearly affected by NQS effects. Note that the simulation model, EKV3, here uses a channel segmentation approach to account for NQS effects [7]. Such an approach ensures compatibility among small-signal frequency-domain and large-signal time-domain simulation. As the present results demonstrate, the five channel segments allow us to represent NQS effects accurately in $L_f = 2 \, \mu m$ devices in all the available frequency range.

The transit frequency $f_t$ of the short-channel devices were evaluated against the drain current, according to,

$$f_t = |H_{21}(f)| \times f_{\text{spot}}, \quad f_{\text{spot}} = 10 \, \text{GHz}$$  \hspace{1cm} (16)

The result in Figure 15 shows that EKV3 can accurately reproduce $f_t$ at all drain voltages $V_D$ for all levels of current and for both NMOS and PMOS devices equally well.

Finally, the scaling abilities of the model in terms of $Y$-parameters are further illustrated in Figures 16.
and 17 for NMOS and PMOS devices, respectively, for the whole range of channel lengths at the median condition of gate and drain bias.

A comment on the appreciation of the overall modelling quality is in order. The overall good qualitative behaviour—bear in mind that single, scalable parameter sets are used to encompass all device characteristics from static to RF and over all geometry and bias conditions—largely outweighs the occasional imperfect fitting.

Investigation of other scaling aspects, such as dependence on varying number of fingers and different finger width, as well as presentation of RF parameter extraction procedures [3, 4, 6, 16], are beyond the scope of the present work and will be presented elsewhere.

V. CONCLUSIONS

In summary, an extended validation of the charge-based EKV3 MOSFET model for analogue/RF IC design has been presented. The EKV3 model was shown to cover qualitatively well all aspects from DC to CV characteristics and RF parameters up to 20 GHz. RF measurements of multi-finger devices include six different channel lengths ranging from 110 nm to 2 μm for both types of transistors (NMOS and PMOS), at about 25 different bias conditions each. Y-parameters were evaluated over different bias conditions and the whole range of channel lengths, and were shown to be well represented by a single, scalable model consistent with the DC and CV results. An overall excellent qualitative fit is achieved with the EKV3 model at all bias conditions and channel lengths over the whole frequency range. Non-quasi static (NQS) effects for long-channel devices are shown to be well addressed at all bias conditions up to 20 GHz, while short-channel devices are more notably affected by the gate and substrate parasitics. Note that such extended validation covering a similarly wide geometry space, bias conditions and type of devices is rarely available in literature and has been shown for the first time for the EKV3 model here. Beyond the abilities of the circuit simulation model, the charge-model approach offers manageable expressions including in terms of RF parameters, and thereby provides significant insight into the operation of the device. This underlines the suitability of the EKV3 MOSFET model for analogue/RF CMOS design. The abilities of EKV3 in terms of scalability using advanced CMOS technology have been largely demonstrated.

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**BIOGRAPHIES**

**Matthias Bucher** was born in Switzerland in 1964. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1993 and 1999, respectively. The subject of his Ph.D. Thesis was the analytical charge-based compact modelling of MOSFETs. In 1997, he was an invited researcher with LSI Logic, Milpitas, California. From 2000 to 2003, he was a visiting researcher at the National Technical University of Athens (NTUA), Athens, Greece, and held numerous consulting mandates in microelectronics industry. In February 2004, he joined the Department of Electronics and Computer Engineering, Technical University of Crete (TUC), Chania, Greece, as an Assistant Professor. His current research interests are in the design of analogue/RF integrated circuits, and in wide-band character-ization and advanced compact modelling of single- and multi-gate nanoscale CMOS as well as high-voltage MOS devices. He also has coordinated the EKV3 MOSFET compact model code development. He is a member of the IEEE and of the Technical Chamber of Greece. He is an author or co-author of over 45 publications in international journals and conferences, as well as of two book chapters.

**Antonios Bazigos** was born in Athens, Greece, in 1980. He received the diploma degree in electrical and computer engineering in 2003 from the National Technical University of Athens (NTUA), Athens, Greece. Since then he is working on his Ph.D. Thesis at the Laboratory of Microelectronics at NTUA. His field of research is the modelling of the MOS transistor.

He is co-working, with the rest of the EKV Team, on the development and the code implementation of the EKV3 MOS transistor compact model.
Sadayuki Yoshitomi was born in Sasebo, Japan, in 1965. He received the B.E., M.E. and Ph.D. degrees from Yokohama National University, Yokohama Japan, in 1988, 1990 and 1993, respectively. The title of his doctor thesis was “Study on the silicon dioxide film deposited by liquid phase deposition (LPD)”. His background is the physics of Si/SiO2 interface.

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Nobuyuki Itoh was born in Tokyo, Japan, in 1960. He received B.S. and M.S. degrees in chemistry from Tokyo University of Science, Tokyo, Japan, in 1983 and 1985 respectively, and he received Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2006. In 1985, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the research and development of CMOS device technologies for advanced CMOS gate arrays, bipolar device technologies and bipolar circuit design for ECL gate arrays and high-frequency analogue circuits, and RF-CMOS circuit design. He was a visiting scientist at Katholieke Universiteit Leuven, ESAT-MICAS, Leuven, Belgium, from March of 1996 to April of 1998 where he worked on design of fully integrated VCOs and PLLs using RF-CMOS. He has been engaged in the research and development of high-frequency analogue circuit at Semiconductor Company of Toshiba Corporation since 1998. His current research interests are high-frequency integrated circuit for telecommunications. Dr. Itoh is a member of the Institute of Electronics and Communication Engineers of Japan (IEICE) and member of the Institute of Electrical and Electronics Engineers (IEEE). He is also a member of program committee of Custom Integrated Circuit Conference (CICC), Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), European Solid-State Circuits Research Conference (ESSCIRC) and Asia-Pacific Microwave Conference (APMC).