Typical Mechanisms in Advanced SOI MOSFETs and Challenging Issues for Compact Modeling

Sorin Cristoloveanu

- Almost no introduction
- Operation of SOI transistors
- Gate tunneling and floating-body effects
- Fringing fields and short-channel effects
- Narrow-channel effects
- Extremely thin film effects
- Self-heating
- Double-gate operation
- Multiple-gate MOSFETs
- Next speaker
**SOI Technology - Definition & Questions**

**Definition:** SOI is a young technology for the future of the microelectronics

- **Is SOI really young?**
  - Yes, 30-35 years only
  - No, twice as old as the lifetime left on ITRS

- **Is SOI for the future?**
  - (Yes)$^2$! Bulk cannot make it. There is nothing left, but SOI!

- **Is the future what it used to be?**
  - No, because SOI allows expanding the frontiers!
Why SOI?

- **Dielectric isolation**: vertical and lateral (no latch-up)
- **Vertical junctions**: reduced leakage and capacitance
- **Excellent tolerance of transient radiation effects**
- **Simpler processing & high flexibility**: no wells or trenches
- **Ideal structure** for sensors, MEMS, high-temperature devices
- **Attenuated short-channel effects**: enhanced scaling
- **Low-voltage & low-power operation**: sharp subthreshold swing, reduced leakage, low $V_T$
Floating-Body Effects in PD SOI MOSFETs

- Kink effect
- Models available!
- Latch & related noise
Fully Depleted MOSFETs: Coupling Effects

(a) $I_D$ vs $V_{G1}$
(b) $\log I_D$ vs $V_{G1}$
(c) $g_m$ vs $V_{G1}$
(d) $V_{T1}$ vs $V_{G2}$
(e) $S_1$ vs $V_{G2}$
(f) $\mu_1$ vs $V_{G2}$
Threshold Voltage Equations

\[ V_{T1} - V_{T1'} = \frac{C_{ox1}}{C_{ox1} + C_{sl} + C_{ox2}} [V_{G2} - V_{acc2}^{cc}] \]

- \( V_{T1}^{dep} = V_{T1}^{acc} - \frac{C_{sl} C_{ox2}}{C_{ox1} (C_{ox2} + C_{sl} + C_{R2})} [V_{G2} - V_{acc2}^{cc}] \)
- slope \( \Rightarrow \frac{1}{L} \frac{dV_{G2}}{dV_{T1}'}, \) and \( D_{R2} \) profile

\[ D_{R2} = \frac{1}{q} \left( \frac{C_{sl} C_{ox2}}{C_{ox1}} \frac{dV_{G2}}{dV_{T1}'} + C_{sl} + C_{ox2} \right) \]

- \( V_{T1}^{acc} - V_{T1}^{dep} = \frac{C_{sl}}{C_{ox1}} \times 2\phi_F \Rightarrow \text{doping} \)
- Reciprocal measurements \( V_{T2} (V_{G1}) \)

Transconductance

\[ I_D = \frac{C_{ox1} W V_D}{L} \mu_{eff} \left( V_{G1} - V_T (V_{G2}) \right) \]

\[ \beta_{m1} = \frac{C_{ox1} W V_D}{L} \times \left[ 1 + \sqrt{1 + \frac{\phi}{V_{G1} - V_T (V_{G2})}} \right] \]

1) Back interface accumulated
   - unique \( \beta_{m1} (V_{G1}) \) curve
   - high vertical field \( \Rightarrow \mu_1 \)

2) Back interface depleted
   - \( \beta_{m1} (V_{G1}) \) depends on \( V_{G2} \)
   - high mobility
   - \( \beta_{max} = \beta_{max1} \left[ 1 - 2(R_1 + R_3) G_{01} \right] \)

3) Back interface from depletion to inversion
   - the back channel opens before the front channel
   \( \Rightarrow \text{transconductance plateau} \Rightarrow \mu_2 \)

4) Back interface always inverted
   - maximum series resistances effect \( (R_1, R_2, R_3) \)
Notes:

- The front channel is sensitive to back-gate bias and quality of BOX and back interface
- Conventional models account for 2-interface coupling
- MOSFETs with thin BOX require 3-interface models and substrate depletion effects
Self-Heating in SOI MOSFETs

Drain current $I_D$ (mA) vs. Drain voltage $V_D$ (V)

Channel temperature $T$ (°C) vs. Power (mW)

$V_{G1} = 5$ V

$t_{si}$ (nm) = 41, 78, 177, bulk Si
Thermal Conductance: Analytical Model

- Thermal equivalent circuit
- BOX contribution prevails
  Change the BOX material!!

Sorin 20-05
Solution: Thin Buried Alumina

Thinner BOX reduces the channel lattice temperature.
The advantage of Al₂O₃ BOX is maintained for thin BOX.
**Gate-Induced Floating-Body Effects (GIFBE)**

A new scaling-related effect:
- FBE induced by gate tunneling
- second peak in transconductance
- time & frequency dependent
- decreases in shorter or narrower channels

Pretet et al'02
GIFBE : Analysis

- The body potential is defined by the balance between gate-to-body current and recombination current
- Suppression of current transients (overshoot & undershoot)
- Impact on history effects in ICs

![Diagram of MOSFET with key points labeled: Gate, Body, Substrate, S, D, BOX.]

![Graph showing normalized drain current vs. time with logarithmic scale for different gate voltages and channel lengths.]

W = L = 10 µm
V_D = 0.1 V

V_G1 : 0 -> 1.2 V
V_G1 : 0 -> 1.1 V
V_G1 : 0 -> 0.9 V

Log(|I_b| (A))
GIFBE: History Effects and Excess Noise

**Inverter Chain:**
- 1st switch slowed down
- 2nd switch accelerated
- Steady-state reached faster


1/f + Lorentzian excess noise
Surprising GIFBE in Fully Depleted MOSFETs

- Second peak even for $V_{G2} = 0$
- More accumulated back interface $\rightarrow$ higher peak

**Model:**

\[
\Delta V_{T1} \approx -\Delta \Psi_{s1} \approx -\frac{C_{si}}{C_{si} + C_{ox1}} \Delta \Psi_{s2} \quad \text{coupling}
\]

\[
I_D \sim (V_{G1} - V_{T1})
\]

\[
g_m = g_{m0} \times \left(1 + \frac{C_{si}}{C_{si} + C_{ox1}} \cdot \frac{\Delta \Psi_{s2}}{\Delta V_{G1}}\right)
\]

**Peak for** $\Delta \Psi_{s2}/\Delta V_{G1} \approx 1$
Scaling of SOI MOSFETs

Models

Intrinsic length $\lambda$. [Yan’92, Monroe ’00]

$$\lambda = (t_{si} \, t_{ox} \, \varepsilon_{si}/\varepsilon_{ox})^{0.5} \quad \text{or}$$

$$\lambda = (t_{si} + t_{ox} \, \varepsilon_{si}/\varepsilon_{ox})/\pi$$

Tolerable short-channel effects for $L_G \approx 3 \lambda$

Message:

- worst case: transition from partial to full depletion
- use ultra-thin FD films $t_{si} = t_{ox} = 1 \text{ nm} \Rightarrow L_G = 5 \text{ nm}$ !!
- doping effect becomes irrelevant: high mobility

[Su’94]
No doping effect below 15 nm!

Fringing Fields in SOI

Medication:
- Thin Si film
- Thin BOX (not too thin!)
- Low-K BOX (SON?)
- Ground-plane (genetics!!)

No doping effect below 15 nm!
Distribution of Fringing Fields in SOI MOSFETs

Analytical model based on conformal mapping

Ernst et al’99
Narrow-Channel Effects in SOI MOSFETs

**Classical effects**: $V_T$, $g_m$ vs. $W$
- Coupling between width, length and thickness
- LOCOS: sidewall overdoping
  less efficient in ultra-thin films
- STI: corner effects
- Models available

**Special SOI Effects**: FBE
- Subthreshold swing increases in narrow & thick (PD) channels
- Attenuated floating-body effects
- No models

[Pretet’01]
Floating-Body Effects in Narrow SOI MOSFETs

**Why are FBE attenuated?**
- Breakdown and snapback voltages increase in narrow channels
- Transients effects are much shorter
- Reduced history effects

**[Pretet’01]**
Chopping the SOI MOSFET's

Volume $\approx 10^{-18} - 10^{-19}$ cm$^3$

- What is the meaning of $10^{17}$ cm$^{-3}$ doping level? 
- Is the impurity location important?
- A few thousands Si atoms, only. Call them by name!
- Modeling and simulation tools
- Statistical fluctuations

Length $\Rightarrow$ 10 nm  
Thickness $\Rightarrow$ 1 nm  
Width $\Rightarrow$ 10 nm
Ultra Thin Film Effects in SOI MOSFETs

Coupling curves $V_{T1}(V_{G2})$ and $V_{T2}(V_{G1})$

Thick film: the two curves intercept
Ultra-thin film: the curves are superposed

$$\Delta V_{T1} \approx -\frac{t_{ox1}}{t_{ox2}} \Delta V_{G2}$$

$$\Delta V_{T2} \approx -\frac{t_{ox2}}{t_{ox1}} \Delta V_{G1}$$

Sorin et al’03
Pseudo-Double-Gate Operation

Similar front and back inversion charges:

\[ V_{G1} - V_{T1} = \frac{t_{\text{ox1}}}{t_{\text{ox2}}} (V_{G2} - V_{T2}) \]

What is the correct value of \( V_{T1} \) and \( V_{T2} \)?

- Thick film: intercept point
- Thin film: any value on the common curve!
- Wrong biasing: unrealistic mobility value

This relation does not apply to weak inversion:
World record: swing 7 mV/dec!!
Ultimately Thin Double-Gate MOSFETs

- 3-nm-thick DG-MOSFET
- simultaneous biasing of front and back gates: $V_{G2} = 1.2 V_{G1}$
- outstanding transconductance gain: up to 400%
- mobility effect rather than charge effect

Impact of volume inversion

Cristoloveanu et al’99
Impact of Volume Inversion on Mobility

- Dimensional confinement: $t_{si} < 10$ nm
- $V_T$ increases below 10 nm
- Quantum charge distribution totally different from classical profile (Poisson)
- Enhanced volume inversion [Sangiorgi et al '98]

- SG: more carriers flow near interfaces
- DG: most carriers flow far from interfaces
  - lower vertical field
  - less roughness-induced scattering
  - empirical model showing mobility gain [Cristoloveanu et al'99]
Carrier Mobility in Ultra Thin SOI MOSFETs

- Monte-Carlo simulations indicate [Gamiz'01]:
  (including phonon + Coulomb + surface roughness scattering)
  - enhanced mobility in sub-10-nm thickness range
  - higher mobility in DG-MOSFETs

- Experiments in MOS-Hall devices demonstrate [Mastrapasqua'01]:
  - improved mobility in recent SOI materials
  - good mobility in sub-10-nm thick MOSFETs
  - higher mobility in DG-MOSFETs

Compact models ??
Ultimate Scaling of DG-MOSFETs

**Intrinsic length $\lambda$**

- Acceptable short-channel effects if $L_G \geq 3 \lambda$

$$\lambda = \left[ \frac{k}{2} t_{si} t_{ox} \right]^{0.5} \quad \text{or} \quad \lambda = \frac{t_{si} + 2kt_{ox}}{\pi} \quad \text{with} \quad k = \frac{\varepsilon_{si}}{\varepsilon_{ox}}$$

- Ultra thin SOI films will be necessary for 10-nm-long DG-MOSFETs

---

Intrinsic length $\lambda$

- Acceptable short-channel effects if $L_G \geq 3 \lambda$

$$\lambda = \left[ \frac{k}{2} t_{si} t_{ox} \right]^{0.5} \quad \text{or} \quad \lambda = \frac{t_{si} + 2kt_{ox}}{\pi} \quad \text{with} \quad k = \frac{\varepsilon_{si}}{\varepsilon_{ox}}$$

- Ultra thin SOI films will be necessary for 10-nm-long DG-MOSFETs

---

**Intrinsic length $\lambda$**

- Acceptable short-channel effects if $L_G \geq 3 \lambda$

$$\lambda = \left[ \frac{k}{2} t_{si} t_{ox} \right]^{0.5} \quad \text{or} \quad \lambda = \frac{t_{si} + 2kt_{ox}}{\pi} \quad \text{with} \quad k = \frac{\varepsilon_{si}}{\varepsilon_{ox}}$$

- Ultra thin SOI films will be necessary for 10-nm-long DG-MOSFETs
Transport Properties in FinFETs

- 4 channels
- 2 gates
- Corners
- Coupling Models ??

Lateral mobility

N-channel
- Lateral interface: 196 cm²/Vs
- Front interface: 677 cm²/Vs
- Back interface: 682 cm²/Vs

P-channel
- Lateral interface: 96 cm²/Vs
- Front interface: 163 cm²/Vs
- Back interface: 150 cm²/Vs

Sorin 20-05
Field-Effect Junctions: Series Resistance Lowering

Accumulation layers:

⇒ Low $R_S$
⇒ Low $R_D$

50-100 Centered

Accumulation layer:

⇒ Low $R_S$
⇒ Improved $g_m$

50-100 Drain

50-100 Source

Allibert et al’01

Sorin 20-05
The 4-Gate Transistor: **\( G^4 - \text{MOSFET} \)**

- **Maximum number of gates!**
- **\( G^4 - \text{MOSFET} = \text{MOSFET} + \text{JFET} \)**
  - 2 lateral junction gates ⇒ JFET mode
  - Front and back gates ⇒ MOSFET mode
- **Standard partially-depleted SOI technology**
- **Depletion/accumulation device**
- **Drawn MOSFET length defines width**
- **MOSFET width defines channel length**

Cross-section view

Cristoloveanu et al’02

Sorin 20-05
$G^4$-MOSFET: Typical Characteristics

N-channel MOS-JFET ($L = 1.5\text{um}, W = 0.35\text{um}$) with $V_{\text{SUBSTRATE}} = 0\text{V}$

- $V_{PG} = 3\text{V}, V_{JG} = 0\text{V}$
- $V_{PG} = 2\text{V}, V_{JG} = 0\text{V}$
- $V_{PG} = 1\text{V}, V_{JG} = 0\text{V}$
- $V_{PG} = 0\text{V}, V_{JG} = -1\text{V}$
- $V_{PG} = 0\text{V}, V_{JG} = -2\text{V}$

$V_{JG} =$ junction-gate voltage
$V_{PG} =$ poly-gate voltage

Front-gate modulation
MOSFET action

Junction-gate
JFET action
**G⁴-MOSFET: Typical Characteristics**

- Current control by either front gate or junction gates
- Back-gate depletion makes easier device cut-off (full depletion)
- Top and back gate accumulation enables large currents
- Applications: mixed signals, low-power modulation, RF mixers
- New logic families: quaternary logic
**G⁴-FET: Modeling**

How can a partially depleted body become fully depleted?
- The doping seen by one gate is lowered by the other gates
- Concept of effective doping
- The depletion region is expanded: the G⁴-FET can be turned off

Mathematical expression:

\[ n(x) = \frac{N_D}{2} \left[ 1 + \text{th} \left( \frac{x - W_D}{\alpha L_D} \right) \right] \]
Advanced SOI MOS scaling:
• ultra-thin gate oxides => new Gate Induced FBEs
• the transistor body will be the thinnest layer
• ultra-thin silicon films => new coupling effects
• thin BOX or other types of BOX => relax self-heating
• double gate transistors: new quantum and transport effects

Other modeling issues: series resistance, thickness fluctuations, quantum effects, mobility behavior, coupling and corner effects, transient and history effects, etc, etc

Do we need a conclusion ??

Context: - SOI is no longer a promising technology
- SOI is the necessary technology

Join the SOI Club !!!