BSIM-IMG: Surface Potential based UTBSOI MOSFET Model

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The Nano-Tera Workshop on the Next Generation MOSFET Compact Models, EPFL, Switzerland.
SPICE Transistor Modeling for Circuit Simulation

- **Simulation Time**
  - ~ 10µs per DC data point
  - No complex numerical method allowed

- **Accuracy requirements**
  - ~ 1% RMS Error after fitting

- **Excellent Convergence**

- **Example: BSIM4**
  - 25,000 lines of C code
  - 200+ parameters
  - Open-source software implemented in all EDA tools
BSIM Family of Compact Device Models

1990

BSIM3


BSIM4

2005

BSIM-MG

2010

BSIMSOI

BSIM6

Conventional MOSFET

Silicon on Insulator MOSFET

Multi-Gate MOSFET

BSIM: Berkeley Short-channel IGFET Model
Versatile Multi-Gate Compact Model: BSIM-MG

BSIM-IMG

UTBSOI
BG-ETSOI

BSIM-CMG

FinFETs on Bulk and SOI Substrates

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Thin-body SOI Devices

UTBSOI
Y. Choi et al.
EDL 2000
(UC Berkeley)

ETSOI
K. Cheng et al.
IEDM 2009
(IBM)

UT2B
F. Andrieu et al.
VLSI 2010
(CEA-LETI)

UTBB
Q. Liu et al.
VLSI 2011
(ST)

Wafer Uniformity (SOITEC):
F. Andrieu et al., VLSI 2010
Executive Summary/ Outline: BSIM-IMG

- Production Ready Compact Model for FDSOI
- Physical Core Model
- Palette of Real Device Effects
- Validated to Hardware Silicon Data
- Synchronized with EDA Vendors Tools

Real Device Effects

Core SPE

I-V C-V

BSIM-IMG Validation
Outline

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- Model Validation & QA
- Future Research
- Conclusion
Independent-gate Device Structure: BSIM-IMG

- Asymmetric structure
  - Different Gate Workfunctions
  - Allows dissimilar Gate Potentials
  - Different Oxide thickness and Material!

- Captures important features
  - Threshold Voltage tuning through Back-Gate
  - Multi-$V_{th}$ technology
Computationally Efficient Core

- Efficient Non-iterative Surface Potential calculation
  - Investigated NR, Shooting Secant etc.

- Surface potential needs to solved at least twice - Source and Drain side
  - Obtain $\psi_s / Q_{is}$ and $\psi_d / Q_{id}$

D. Lu et al., SSE 2011
Surface Potential Derivation

- Quasi-Fermi level at the source is taken as a reference for the potential ($\psi$).

$$\psi = -\frac{E_c - E_f(\text{source})}{q}$$

- Start from the Poisson’s equation

$$\varepsilon_{si} \frac{d^2 \psi(x,y)}{dx^2} = qN_c \exp \left( \frac{q(\psi(x,y) - V_{ch}(y))}{kT} \right)$$

- The continuity of displacement field at the front and back interfaces gives the following relation of the surface electric fields ($E_{s1} = -\frac{d\psi}{dx}\bigg|_{x=-Tsi/2}$ and $E_{s2} = -\frac{d\psi}{dx}\bigg|_{x=Tsi/2}$) and surface potentials:

$$C_{ox1(2)} (V_{fg(bg)} - \Delta \Phi_1(2) - \psi_{s1(2)}) = \varepsilon_{si}E_{s1(2)}$$
Surface Potential Derivation (Contd.)

- Multiplying both sides of Poisson’s Eq. by $\frac{d\psi}{dx}$ and integrating yields

$$E_{s1}^2 - E_{s2}^2 = \frac{2qN_iV_{th}}{\varepsilon_{si}} \left\{ \exp\left(\frac{\psi_{s1} - V_{ch}}{V_{th}}\right) - \exp\left(\frac{\psi_{s2} - V_{ch}}{V_{th}}\right) \right\}$$

- Replacing $E_{s1}$ with $\psi_{s1}$

$$\left(\frac{C_{ox1}(V_{fg} - \Delta \Phi_1 - \psi_{s1})}{\varepsilon_s}\right)^2 - E_{s2}^2 = \frac{2N_c kT}{\varepsilon_{si}} \exp\left(\frac{q(\psi_{s1} - V_{ch})}{kT}\right)$$

- $E_{s2}$ approximation

$$E_{s2} = \left(\frac{V_{fg} - \Delta \Phi_1}{\varepsilon_{sox}(T_{ox1} + T_{ox2}) + T_{si}}\right)\tfrac{\varepsilon_{si}}{\varepsilon_{sox}}(T_{ox1} + T_{ox2}) + T_{si}$$

- Using perturbation to improve accuracy at strong inversion

$$E'_{s2} = \psi_{s1}^{(1)}\left(\frac{V_{bg} - \Delta \Phi_2}{\varepsilon_{si}T_{ox2} + T_{si}}\right)$$
Relating $\psi_{s2}$ with $\psi_{s1}$

Generalization of Poisson's equation

$$\left( \frac{d\psi}{dx} \right)^2 - A \cdot \exp \left( \frac{q(\psi - V_{ch})}{kT} \right) = D$$

**$D < 0$**

$$t_{01} = \left( \frac{2kT}{q\sqrt{-D}} \right) \cos^{-1} \left[ \sqrt{\frac{D}{A}} \exp \left( -\frac{q(\psi_{s1} - V_{ch})}{kT} \right) \right]$$

$$t_{02} = \begin{cases} |T_{si} - t_{01}| & E_{s1} > 0 \\ T_{si} + t_{01} & E_{s1} < 0 \end{cases}$$

$$\psi_{s2} = V_{ch} - \frac{kT}{q} \ln \left\{ \frac{A}{-D} \cos^2 \left( \frac{q\sqrt{-D}}{2kT} t_{02} \right) \right\}$$

**$D > 0$**

$$\psi_{s2} = V_{ch} + \frac{kT}{q} \ln \left[ \frac{D}{A} \left( \frac{2C}{1-C^2} \right)^2 \right]$$

$$C = \left[ \sqrt{\frac{D}{A}} \exp \left( -\frac{q(\psi_{s1} - V_{ch})}{kT} \right) + 1 \right] - \sqrt{\frac{D}{A}} \exp \left( -\frac{q(\psi_{s1} - V_{ch})}{kT} \right)$$

$$\times \exp \left[ -\text{sgn}(E_{in}) \frac{q\sqrt{D}}{2kT} t_{01} \right]$$

$E_{s2} = -\frac{\partial \psi_{s2}}{\partial t_{01}}$

$Q_{inv} = \epsilon_s (E_{s1} - E_{s2})$
Surface Potential: Verification with TCAD

Scalable w.r.t. physical parameters like $T_{si}$, $T_{ox}$ (front and back) and node voltages etc.
Volume Inversion

- **Preserves Important Property** like Volume Inversion
  - In sub-threshold (Low field), the charge density $Q_i$ is proportional to the body thickness $T_{si}$

$T_{oxb} = 10\mu$m

![Graph showing charge density and front surface potential](image)
Drain Current Model

- **Drain Current**

\[
I_{ds} = \mu \cdot \frac{W}{L} \cdot \left[ \frac{Q_{inv,s} + Q_{inv,d}}{2} \left( \psi_{s1,d} - \psi_{s1,s} \right) + \eta \cdot \frac{kT}{q} \left( Q_{inv,s} - Q_{inv,d} \right) \right]
\]

\[
\eta = 2 - \frac{2\varepsilon_{si}E_{s2}}{Q_{inv} + 2\varepsilon_{si}E_{s2}}
\]

**No Charge-sheet Approximation**

- **Drift**
- **Diffusion**

- \(Q_{inv}\): inversion carrier density
- \(E_{s2}\): back-side electric field
- \(\psi_{s1}\): front-side surface potential

**Very high accuracy**

![Graphs showing comparison between Charge-sheet Model, This Work, and TCAD.](image)
Capacitance Model

- Model inherently exhibits symmetry
  - \( C_{ij} = C_{ji} \quad @ \quad V_{ds} = 0 \text{ V} \)
- Model overlies TCAD results
  - No tuning parameters used

Symbols: TCAD Results; Lines: Model

\( T_{oxf} = 1.2\text{nm}, \ T_{oxb} = 20\text{nm}, \ T_{si} = 15\text{nm}, \ V_{bg} = 0 \text{ V} \)
Outline

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Short Channel Effects

\[ \Delta V_{th} = \frac{0.5 \cdot DVT0}{\cosh \left( DVT1 \cdot \frac{L}{\lambda} \right)} \times (V_{bi} - \phi_s) + \frac{0.5 \cdot ETA0}{\cosh \left( DSUB \cdot \frac{L}{\lambda} \right)} \times V_{ds} \]

Scale Length

\[ \lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \cdot T_{si} \cdot T_{ox1} \cdot \left[ 1 + \frac{T_{ox2} - T_{ox1}}{T_{ox1} + T_{ox2} + T_{si} \cdot \varepsilon_{ox} / \varepsilon_{si}} \right]} \]

Symbols: TCAD
Lines: Model

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Doping Dependence

- Threshold voltage shift as function of doping is captured

![Graph showing doping dependence with labeled axes and data points for different doping concentrations.](Image)
Length Dependent $\gamma$ Model

- Capacitive coupling ratio

$$\gamma = -\frac{dV_{TH}}{dV_{bg}}$$

![Graph showing Capacitive coupling ratio](image)

- $\gamma$ degraded at short channel

![Diagram of transistor model](image)

- $T_{si}=8\text{nm}$
- $T_{box}=4\text{nm}$

Captures $V_{bg}$ effect in I-V
QM Effect: Inv. Charge Centroid Model

\[ V_{dd} = 0.9 \text{ V} ; \ V_{fb} = 28 \text{ mV} \]
\[ T_{\text{BOX}} = 140\text{nm}; \ T_{\text{si}} = 6\text{nm}; \ N_{\text{sub}} = 1e16 \text{ cm}^{-3} \]

\[ E_{\text{OT,phys}} = 0.65\text{nm} \]
\[ T_{\text{inv}} = 1.13\text{nm} \]
\[ E_{\text{OT,eff}} = 0.95\text{nm} \]
Self Heating Model

- **Thermal Node**: $R_{th}/C_{th}$ methodology

- Relies on **Accurate** physical modeling of **Temperature Effects** in the model

\[
R_{th} = \frac{RTH0}{WTH0 + W_{eff}}
\]

\[
C_{th} = CTH0 \cdot (WTH0 + W_{eff})
\]

![Diagram of self heating model with temperature node and physical modeling](image)
Real Device Effects

- Channel Length Modulation and DIBL
- Velocity Saturation
- GIDL Current
- Impact Ionization current
- Direct tunneling gate current
- S/D Resistance/Parasitic Resistance
- Fringe Capacitances
- Overlap capacitances
- Noise models
- More Effects?
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Validation to Hardware Data

Device from CEA-LETI
- $T_{\text{box}} = 145 \text{nm}$, $EOT = 1.6 \text{nm}$, $T_{\text{si}} = 8 \text{nm}$, $W = 0.5 \text{um} \times 50$
- $L = 50 \text{nm}$, $N_a = 1e15$, $\Phi_{g2} = 5.0$, $\Phi_{g1} = 4.55$ (fitted)
- $V_{\text{bg}} = \text{floating, 10V, 15V, 20V, 25V}$

![Graphs showing drain current vs. gate voltage for different $V_{\text{bg}}$ values and BSIM-IMG model comparisons.](image-url)
Validation Contd.

**$G_{m,lin}$**

Cross: Measurements
Lines: BSIM-IMG

$W = 50 \times 0.5 \mu m$
$L = 50 \text{ nm}$

**$I_{d,\text{sat}}$**

$W = 50 \times 0.5 \mu m$
$L = 50 \text{ nm}$

$V_{bg} = 10 \text{v}, 15 \text{v}, 20 \text{v}, 25 \text{v}$

**$I_{d,\text{sat}}$**

Cross: Measurements
Lines: BSIM-IMG

$V_{bg} = 10 \text{v}, 15 \text{v}, 20 \text{v}, 25 \text{v}$

**$G_{m,\text{sat}}$**

Cross: Measurements
Lines: BSIM-IMG

$W = 50 \times 0.5 \mu m$
$L = 50 \text{ nm}$

Increasing $V_{bg}$
Extraction Results: $I_d - V_{fg}$ and $G_m - V_{fg}$ with varying $V_{bg}$

- $I_d - V_{fg}$ with varying back bias
  - $V_{bg} = 0, -0.2, -0.5, -0.8, -1.1$ V
  - $V_{ds} = 50$ mV

- Transconductance ($G_m$)

Lg=30nm TBOX=10nm
Extraction Results: $I_d$-$V_{ds}$ and $G_{ds}$-$V_{ds}$ with varying $V_{bg}$

- $I_d$-$V_{ds}$ at $V_{fg} = 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1$ V
- Output Conductance ($G_{ds}$)

$Lg=30$nm, $TBOX=10$nm
Global Parameter Extraction for ETSOI

- **Calibration of the model**
  - Through internship **at IBM T.J. Watson**
    - Work by Darsen Lu
  - Global Extraction performed for NMOS & PMOS at L=24nm ...... 66nm
  - Excellent agreement for I-V across all gate lengths
  - C-V extracted and fine-tuned to match ring oscillator delay v.s. $V_{dd}$
Gummel Symmetry Test

- **Drain Current Symmetry**

- **AC (charge) Symmetry**

Analog /RF Ready

C. C. McAndrew, TED 2006
Convergence Tests

- Excellent Convergence Properties
- Ex: 17-stage ring oscillator

Various Back-Gate Potential Conditions

\( V_{\text{bgn}} = 0 \text{ V} \)
\( V_{\text{bgp}} = 1 \text{ V} \)

\( V_{\text{bgn}} = -3 \text{ V} \)
\( V_{\text{bgp}} = 4 \text{ V} \)
## Speed Tests

<table>
<thead>
<tr>
<th>Circuit</th>
<th># MOSFETs</th>
<th>Model</th>
<th>Runtime per iteration per transistor (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-Transistor Id-Vds</td>
<td>1</td>
<td>BSIM4 IMG</td>
<td>40.7          29.1</td>
</tr>
<tr>
<td>17-Stage Ring</td>
<td>34</td>
<td>BSIM4 IMG</td>
<td>31.3          18.8</td>
</tr>
<tr>
<td>Coupled Rings</td>
<td>2020</td>
<td>BSIM4 IMG</td>
<td>41.0          22.6</td>
</tr>
</tbody>
</table>

- Speed of BSIM-IMG v101 and BSIM v4.5 compared
  - Both model compiled with the in-built Verilog-A compiler of HSpice
  - Note: Each model uses its own default parameter. Parameters are not extracted for a real technology.
  - GIDL, I_g, Self-heating turned off.

Averaged over 5 runs on a Linux box with a single-core AMD Opteron Processor (2.39GHz)
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Application Example: FinFET SRAM with Backgate Dynamic Feedback

- 6T SRAM Cell using FinFETs

![6T SRAM Cell diagram](image)

- SNM improvement reported based on TCAD mixed-mode simulation.

BSIM-IMG Simulation of FinFET SRAM

- FinFET-based SRAM cells are simulated using BSIM-CMG and BSIM-IMG.
- Back-gate dynamic feedback enhances the read margin from 150mV to 212mV.
- Back-channel inversion required to simulate write margin.

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**FinFET (BSIM-MG)**
- \( L_g = 22 \text{ nm}, \) \( NF=2 \)
- \( I_{off} = 0.05 \mu A / \mu m \)
- **Read Margin**:
  - Without Dynamic FB: 150mV
  - With Dynamic FB: 212mV

**Bulk (PTM 32nm)**
- \( W/L = 75nm / 32nm \)
- **Read Margin**:
  - \( \beta = 1.5 \): 80mV
  - \( \beta = 2.0 \): 101mV

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**Graphs**

- **PD Number of Fingers**
- **Read Margin (mV)**
- **\( \beta \)-ratio**

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*Darsen Lu* - 35
On-going research

- With a high back-gate bias, the double-gate SOI can enter depletion mode
  - Much higher leakage
  - But higher speed!

Symbols: TCAD

Lines: New BSIM-IMG with a novel iterative technique to compute the surface potential

- Lg=10μm
- Tox=1nm, Tsi=8nm, Tbox=20nm
- FG: midgap WF; BG: P+ WF
Where Are We!

- Introduction
- Core Model
  - Surface Potential Equation
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Technology Transfer

  - Available in EDA tools: SimuCAD, ProPlus, Accelicon
  - Implementation **In Progress @** Cadence, Synopsys
  - Package Ready for Technology Evaluation and Design under NDA
    - Verilog-A code and Well-documented Technical Manual
    - Provide **some support and Commitment** to improve the model
Summary

- **BSIM-IMG** is a **Turnkey, Production Ready** model
  - Is submitted to the CMC for standardization
- Physical, Scalable Core Model for FDSOI devices
- Plethora of Real Device Effects modeled
- Advanced Device Effects – Quantum, Back-gate bias
- **Validated** on Hardware Data from two FDSOI/UTBSOI technologies
- Available **in major EDA tools**
Publications & Useful References


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- **Funding**
  - SRC Task 2055
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- **Data**
  - LETI-SOITEC
  - IBM

- **Feedback**
  - EDA Vendors and Users