MOSFET Modeling for Ultra Low-Power RF Design

T. Taris, H. Kraïmia, JB. Begueret, Y. Deval

Bordeaux, France

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Context

More services in...

- Environment survey
- Energy management
- Process optimisation
- Aging follow up
- Localisation service
- Health monitoring
- Human to machine interaction
- Item tracking
- ...
Context

Challenges

- Environment survey
- Energy management
- Aging follow up
- Health monitoring
- Human to machine interaction
- Item tracking

- Low cost
  Price/node <1$
- Small form factor
  1 cm³
- Low power
  Run 10 years!

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Challenges

- Environment survey
- Energy management
- Process optimisation
- Aging follow up
- Localisation service
- Wireless Sensor Networks
- Health monitoring
- Item tracking
- Human to machine interaction
- ...

Low cost

Small form factor

Low power

Run 10 years!

Price/node <1$

1 cm³

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**Context**

**WSN Node Basics**

- **Data processing**
  - Computation
  - Memory writing/reading...

- **Radio module**
  - Data broadcasting
  - Communications

- **Power Unit**
  - Supply
  - Energy Management/Storage

- **Sensor/Actuator**
  - Environment Interface

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WSN Node Basics

- **Radio module**
  - Data broadcasting
  - Communications

- **Sensor/Actuator**
  - Environment Interface

- **Power Unit**
  - Supply
  - Energy Management/Storage

Large Power Consumption

WSN node in Rx mode most of the time
Various approaches to improve the power saving in Radio

Transistor & System Level

Compact RF Demodulator

Compact RFFE Demodulators

RF

Targeted Area

Optimum biasing

Circuit technique

Demod Concept

Compact RFFE

ULP LNA, Mixer,…

LNC, SOM,…

RF Performances

Power Consumption

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Various approaches to improve the power saving in Radio

**Radio Circuit/System Considerations**

- **Transistor Level**
  - LNA
  - Mixer
  - LO
  - Transistor & System Level

- **System Level**
  - Compact RF Demodulator
  - Data

- **Standalone Building Blocks**

**Building Block Combination**

**Targeted Area**

- Optimum biasing
- Circuit technique

**RF Performances**

- Compact RFFE
- Demod Concept
- LNC, SOM...

**Power Consumption**

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OUTLINE

- Context

- From analog to RF Metric

- Low Noise Amplifier Implementation

- Conclusions & Perspectives
Voltage Amplifier

\[ \text{GBW} = A_v \cdot \text{BW} \]

**Figure Of Merit for Low Power amplifier**

\[ FOM_{LPamplifier} = \frac{\text{GBW}}{I_D} \]
From analog to RF Metric

Low Power Analog Amplifiers

Voltage Amplifier

\[ GBW = A_v \cdot BW \]

Configurations

\[ GBW = \frac{g_m}{2\pi C_L} \]

\[ GBW = \frac{g_m}{2\pi C_{gs}} \cdot \frac{r_{ds}}{R_S} \]

Figure Of Merit for Low Power amplifier

\[ FOM_{LPamplifier} = \frac{GBW}{I_D} \propto \frac{g_m}{C.I_D} \Rightarrow \frac{g_m}{I_D} \]
Figure Of Merit for Low Power Analog

\[ FOM_{LP_{\text{analog}}} = \frac{g_m}{I_D} \]

Maximum in WI region

\[ FOM_{LP_{\text{analog}}} \text{ is maximum in WI region} \]
From analog to RF Metric

Low Power RF Circuits

RF Building Blocks

LNA

Mixer

Oscillator

System Level

FOM

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From analog to RF Metric

Low Power RF Circuits

RF Building Blocks

- LNA
- Mixer
- Oscillator

Topologies / Architectures

- Single or diff.
- Active or Passive
- Harmonic or Relax

System Level

\[ FOM_{RFBlock} \propto \frac{g_m}{I_D} \]

Transistor Level

- Cascode
- Common gate
- Common source
- Single device
- Fully or Single balanced
- Cross Coupled LC
- RC oscillator
- Ring oscillator

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Low Noise Amplifier

- A large voltage gain $G_v$ at $f_{RF}$
- A low noise figure $NF$ at $f_{RF}$

Figure Of Merit for Low Power LNA

$$FOM_{LPLNA} = \frac{G_v \cdot f_{RF}}{(F - 1)P_{cons}}$$

System Level

Transistor Level

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From analog to RF Metric

Low Power RF LNA

Low Noise Amplifier

Topologies / Architectures

- Most important characteristics
  - A large voltage gain $G_v$ at $f_{RF}$
  - A low noise figure $NF$ at $f_{RF}$

- Figure Of Merit for Low Power LNA

$$FOM_{LPLNA} = \frac{G_v \cdot f_{RF}}{(F-1) \cdot P_{cons}}$$

System Level

Transistor Level
From analog to RF Metric

Low Power RF LNA

Low Noise Amplifier

- Most important characteristics
  - A large voltage gain $G_v$ at $f_{RF}$
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- Figure Of Merit for Low Power LNA

$$FOM_{LPLNA} = \frac{G_v \cdot f_{RF}}{(F-1) \cdot P_{\text{cons}}(f_{RF})}$$

Common Source Analysis

- $G_v$ at $f_{RF}$
- $P_{\text{cons}} \propto I_D$
- $F_{\text{min, MOS}} \propto 1 + \frac{1}{g_m \cdot R_s}$

System Level

$FOM_{LPLNA, MOS} \propto \frac{g_m \cdot f_T}{I_D}$

Transistor Level
Figure Of Merit for low power LNA

Transductor gain of the device

$FOM_{LP_{LNA}} = \frac{g_m \cdot f_T}{I_D}$

Cutoff frequency of the device

Current consumption

Maximum in MI region

$FOM_{LP_{LNA}}$ is maximum in MI region
OUTLINE

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Ultra Low Power LNA

2.4 GHz LNA - CMOS 0.13μm

440μW@0.5V

→ MOS device in MI region to maximise $FOM_{LPPLNA}$

→ Bulk forward biasing to reduce $V_{th}$
Ultra Low Power LNA

Forward Body Biased Cascode LNA

2.4 GHz LNA - CMOS 0.13µm

Gain & NF vs Power Consumption

→ Limited value on Si

Peaking Load
Ultra Low Power LNA

2.4 GHz LNA - CMOS 0.13µm

Forward Body Biased Cascode LNA

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Ultra Low Power LNA

**Forward Body Biased Cascode LNA**

**2.4 GHz LNA - CMOS 0.13µm**

Gain & NF vs Power Consumption

\[ i_d = \left( \frac{f_T}{f} \right) \frac{1}{R_s \sqrt{1 + (2\pi f R_s)^2}} \]

\( \Rightarrow \) Inductive Degeneration

\( \Rightarrow \) Limited value on Si

Peaking Load

\( \Rightarrow \) Only 6.8 dB@250µW!
Ultra Low Power LNA

Forward Body Biased Cascode LNA

2.4 GHz LNA - CMOS 0.13µm

Gain & NF vs Power Consumption

\[ \text{Gain} \\
\text{NF} \]

\[ \begin{align*}
0.5 \text{V} & \quad \text{Lpk} \\
C_m2 & \quad \text{out} \\
M2 & \quad C_m3 \\
\end{align*} \]

\[ \text{S}_21 \quad \text{NF} \]

\[ \text{f}_T \text{ decrease} \]

\[ \text{Only 6.8 dB@250µW!} \]

\[ \text{Inductive Degeneration} \]

\[ \text{Peaking Load} \]

\[ \text{Limited value on Si} \]

\[ \begin{align*}
0.3 \text{V} & \quad \text{V}_{\text{in}} \\
L_g & \quad \text{R}_{\text{pol}} \\
\text{V}_{\text{pol}} & \quad \text{L}_s \\
\end{align*} \]

\[ \frac{i_d}{v_{\text{in}}} = \frac{f_T}{f} \frac{1}{R_s \sqrt{1 + (2\pi f R_s)^2}} \]

\text{Strong Inversion Techniques}

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Select the best suited topology

➢ To compensate for the low $g_m$ in MI region…

...active load configurations are preferred!
Comparison of the Gain BandWidth (GBW) product…

…the one of self biased inverter is the largest!
Ultra Low Power LNA

Current reuse LNA

2.4 GHz LNA - CMOS 0.13μm

Transistors are in MI region to maximise $FOM_{LPLNA}$

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Ultra Low Power LNA

2.4 GHz LNA - CMOS 0.13µm

Current reuse LNA

100µW@0.5V

4.8dB NF

15dB gain

LNA core

buffer
Ultra Low Power LNA

Current reuse LNA

2.4 GHz LNA - CMOS 0.13µm

Gain & NF vs Power Consumption

100µW@0.5V

Still 13.4dB@60µW!
Ultra Low Power LNA

2.4 GHz LNA - CMOS 0.13µm

Gain & NF vs Power Consumption

100µW@0.5V

Capacitive feedback

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Ultra Low Power LNA

2.4 GHz LNA - CMOS 0.13µm

Gain & NF vs Power Consumption

100µW@0.5V

Current reuse LNA

Capacitive feedback

Still 13.4dB@60µW!

Suited for MI operation
Ultra Low Power LNA

Comparison with the state of art

\[ FOM_{LNA} = \frac{G_v|_{abs}}{P_{DC}(\mu W)} \times \frac{(F-1)|_{abs}}{P_{cons}(mW)} \times \frac{f_{RF}(GHz)}{IIP_3(mW)} \]

Ultra Low Power LNA

Comparison with the state of art

This work ⇒ Cascode

\[ FOM_{LNA} = \frac{G_v|_{\text{abs}}}{{(F - 1)}|_{\text{abs}}} \times \frac{IIP_3|_{\text{mW}}}{P_{\text{DC}}} \times \frac{f_{\text{RF}}|_{\text{GHz}}}{{P_{\text{cons}}|_{\text{mW}}}} \]

\[ (g_m f_T/I_D)_{\text{max}} \]

Ultra Low Power LNA

Comparison with the state of art

\[ FOM_{LNA} = \frac{G_{v,abs} \times IIP_{mW} \times f_{RF,GHz}}{(F-1)_{abs} \times P_{cons,mW}} \]

- **This work ⇒ SBI**
- **This work ⇒ Cascode**

OUTLINE

▪ Context

▪ From analog to RF Metric

▪ Low Noise Amplifier Implementation

▪ Conclusions & Perspectives
Conclusions & Perspectives

RF Building Block Design Methodology

Case of study ➔ LNA

- Capacitive divider ➔ RF Circuit technique
- Self Biased Inverter ➔ Best suited topology
- Active Device biasing ➔ FOM$_{RFblock}$
- MI region ➔ FOM$_{LPLAN}$

Optimize FOM vs Power

\[
FOM_{LPLAN} = \frac{G_{V,S} f_{RF}}{(F-1) P_{cons}}
\]

\[
FOM_{LPLAN|\text{MOS}} \propto \frac{g_m f_T}{I_D}
\]
Conclusions & Perspectives

RF Building Block Design Methodology

To do ➔ Mixer, Oscillator...

- RF Circuit technique
- Circuit performances
- FOM<sub>RFblock</sub> @ circuit
- Best suited topology
- FOM<sub>RFblock</sub> @ transistor
- Active Device biasing

Optimize FOM vs Power

65nm ➔ 28nm

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Conclusions & Perspectives

RF CMOS biasing in future nodes

FOM\textsubscript{RFblock@transistor} versus technology scaling?

FOM\textsubscript{LPLNA}=g\textsubscript{m}.f\textsubscript{T}/I\textsubscript{D}

OR

A matter of Device Modelling